REMARKS

Applicants appreciate the continued thorough examination of the present application and the Examiner's indication that the earlier rejections have been withdrawn. Applicants also appreciate the Examiner's new citation of U.S. Patent 5,512,507 to Yang et al. and U.S. Patent 5,538,917 to Kunitou. Applicants respectfully request reconsideration of these rejections, however, because Applicants will show that the claim recitation of thermal oxide is, in fact, a structural recitation that defines new structures that are not described or suggested in either of the cited references.

In particular, after rejecting the pending claims based on Yang et al. and Kunitou, the final Official Action states at Page 4:

> Regarding the limitation "thermal oxide..." and "buried doping..." (claims 14 and 20), such limitation does not further define the structure as instantly claimed, nor serve to distinguish over Yang and Kunitou. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw make clear.

Applicants respectfully submit that the claimed thermal oxide layer is structurally different than a chemical vapor deposited silicon dioxide layer as described in the cited references, so that the claims are not "product by process" claims. As requested by the Examiner, Applicants will now supply the burden of proof.

The Applicants respectfully refer the Examiner the widely used textbook by Wolf and Tauber, entitled *Silicon Processing for the VLSI Era, Volume 1: Process Technology*. Chapter 6, entitled "Chemical Vapor Deposition of Amorphous and Polycrystalline Thin Films", at Pages 182 and 183 (copy attached), provides a

description of Chemical Vapor Deposited (CVD) silicon dioxide (SiO_2) and its properties compared to thermal silicon dioxide.

Table 2, at Page 183, is entitled "Properties of CVD and Thermal Silicon Dioxide". Applicants respectfully submit that the very fact that these two different silicon dioxides are illustrated as having different properties proves that they are two different materials. Moreover, as noted, "CVD silicon dioxide may have lower density and slightly different stoichiometry from thermal silicon dioxide, causing changes in the chemical and electrical film properties (such as index of refraction, etch rate, stress, dielectric constant and high electric field breakdown strength)". Moreover, page 183 also notes:

> Depending on the deposition conditions, as summarized in Table 2, CVD silicon dioxide is an amorphous structure of SiO_4 tetrahedra with an empirical formula SiO_2. (Emphasis added.)

Finally, Chapter 7 of this textbook, entitled "Thermal Oxidation of Single Crystal Silicon" notes at Page 200 (copy attached):

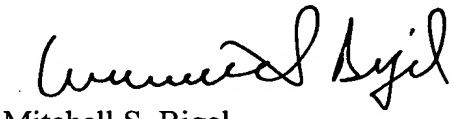
> SiO_2 films grown by the oxidation of silicon, have an amorphous structure with a random network of polyhedra. (Emphasis added.)

This provides additional proof that "thermal SiO_2" is a structural recitation, not a process recitation. For the convenience of the Examiner, Applicants have attached the above-quoted pages of the Wolf et al. textbook, although Applicants are confident that the Examiner already has a copy.

For at least these reasons, Applicants respectfully submit that the use of the term "thermal oxide" in the pending claims is a structural limitation that distinguishes the pending claims over the cited references. For the sake of completeness, Applicants also wish to note that the Yang et al. reference clearly describes the use of CVD silicon dioxide directly on the sidewall of a first planar conductive layer pattern, as noted in the passage cited by the Official Action (Column 4, lines 21-26). Moreover, Kunitou does not describe or suggest a first planar conductive layer pattern including a sidewall but, rather, describes a continuous polysilicon film **12** that does not include sidewalls. Finally, Applicants wish to note that "buried doping" is used to define doping beneath the surface of the integrated circuit substrate, as reflected in the claim recitation "beneath the thermal oxide layer".

In view of the above, Applicants respectfully request withdrawal of the outstanding rejections and allowance of the present application.

Respectfully submitted,



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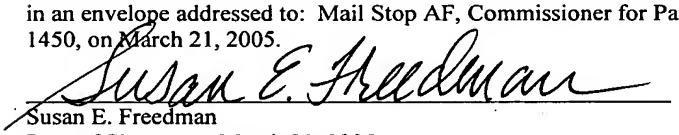

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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boundaries, dopant redistribution and activation of implanted polysilicon can be achieved by RTP in less than 30 seconds at 1150°C. The advantage of using RTP is its short duration, which avoids redistributing dopants in the single crystal silicon substrate. Note that ion implantation of poly-Si with As, followed by a rapid-thermal processing step, has also been investigated as a method for forming shallow emitters in advanced bipolar technologies.

In Situ Doping of Polysilicon

In situ doping involves adding doping gases such as diborane and phosphine to the CVD reactant gases[50]. Although combining doping and deposition in one step may appear simple, the control of film thickness, dopant uniformity, and deposition rate is greatly complicated by the addition of the dopant gases. Moreover, the physical properties of the film are affected. Adding phosphine can change the temperature dependence of the polycrystalline film structure, grain size, and grain orientation. In undoped films, it is reported that depositing an initially amorphous film results in superior structural perfection after anneal[21]. Note that for *in-situ* arsenic or phosphorus doped poly-Si, an oxide capping layer must either be deposited or thermally grown before or during the anneal cycle, in order to avoid outdiffusion of the dopant through the top surface of the polysilicon during the anneal. If the deposition temperature is high enough (>600°C) to result in an as-deposited polycrystalline film with sufficiently low resistivity, then the high temperature anneal step may be skipped altogether.

Oxidation of Polysilicon

Polysilicon, like single crystal silicon, can be thermally oxidized. Its oxidation rate depends on grain orientation, dopant type, and dopant concentration. In general, lightly doped poly-Si oxidizes more rapidly in wet O_2 than {111} or {100} single crystal silicon[29]. Polysilicon heavily-doped with phosphorus oxidizes more rapidly than undoped poly-Si, but not as rapidly as heavily-doped single crystal Si[28]. The ratio of poly-Si consumed during oxidation, to the thickness of the oxide, is about the same as in single-crystal Si (1:1.56).

Of particular importance in some applications (especially in which a double-poly, or even triple-poly structure is used) is that SiO_2 thermally grown on the poly-Si exhibits adequate breakdown strength. This strength is strongly influenced by the smoothness of the polysilicon surface prior to oxidation. That is, a rough surface leads to high local electric fields and lower oxide dielectric strength. Again, low temperature poly-Si depositions (<600°C) have been reported to produce smoother surfaces and grown oxides with higher breakdown voltages than obtained under higher temperature depositions. Another technique reported to increase the smoothness of the poly-Si /SiO_2 interface is to grow the oxide at higher temperatures. It is believed that the viscous flow of the oxide can moderate the surface roughness produced by oxidation. A method for reducing leakage and increasing the breakdown strength of oxides grown on phosphorus-doped poly-Si is to dope it to an optimum level (~6×10^{20} cm^{-3}), with a high temperature anneal in an inert ambient (~1100°C, 10 min, N_2) prior to a 950°C oxidation[30]. This is thought to improve interface flatness by phosphorus-enhanced grain growth during the anneal.

PROPERTIES AND DEPOSITION OF CVD SiO_2

Chemical vapor deposited (CVD) SiO_2 films, and their binary and ternary silicates, find wide use in VLSI processing. These materials are used as insulation between polysilicon and metal layers, between metal layers in multilevel metal systems, as getters, as diffusion sources, as diffusion and implantation masks, as capping layers to prevent outdiffusion, and as final

Table 2. PROPERTIES OF CVD AND THERMAL SILICON DIOXIDE[1]

FILM TYPE:	THERMAL	PECVD	APCVD	$SiCl_2H_2+N_2O$	TEOS
Deposition Temp. (°C):	800-1200	200	450	900	700
Step Coverage:	conformal	good	poor	conformal	conformal
Stress ($x10^9$ dynes/cm^2):	3C	3C-3T	3T	3T	1C
Dielectric Strength (10^6 V/cm):	3 - 6	8	10	10	
Etch Rate (Å /min): (100:1, H_2O:HF)		400	60	30	30

passivation layers. In general, the deposited oxide films must exhibit uniform thickness and composition, low particulate and chemical contamination, good adhesion to the substrate, low stress to prevent cracking, good integrity for high dielectric breakdown, conformal step coverage for multilayer systems, low pinhole density, and high throughput for manufacturing.

CVD silicon dioxide is an amorphous structure of SiO_4 tetrahedra with an empirical formula SiO_2. (See Chap. 7, section on *Properties of Silica Glass.*) Depending on the deposition conditions, as summarized in Table 2, CVD silicon dioxide may have lower density and slightly different stoichiometry from thermal silicon dioxide, causing changes in mechanical and electrical film properties (such as index of refraction, etch rate, stress, dielectric constant and high electric-field breakdown strength). Deposition at high temperatures, or use of a separate high temperature post-deposition anneal step (referred to as *densification*) can make the properties of CVD films approach those of thermal oxide.

Deviation of the CVD silicon dioxide film's refractive index, n, from that of the thermal SiO_2 value of 1.46 is an often used as an indicator of film quality. A value of n greater than 1.46 indicates a silicon rich film, while smaller values indicate a low density, porous film. CVD SiO_2 is deposited with or without dopants, and each type has unique properties and applications.

Chemical Reactions for CVD SiO_2 Formation

There are various reactions that can be used to prepare CVD SiO_2. The choice of reaction is dependent on the temperature requirements of the system, as well as the equipment available for the process. The deposition variables that are important for CVD SiO_2 include: temperature, pressure, reactant concentrations and their ratios, presence of dopant gases, system configuration, total gas flow, and wafer spacing. There are three temperature ranges in which SiO_2 is formed by CVD, each with its own chemical reactions and reactor configurations. These are: 1) low temperature deposition (300-450°C); 2) medium temperature deposition (650-750°C); and 3) high temperature deposition (~900°C).

The *low temperature deposition* of SiO_2 utilizes a reaction of silane and oxygen to form undoped SiO_2 films. The depositions are carried out in APCVD reactors (primarily of the continuous belt type), in distributed feed LPCVD reactors, or in PECVD reactors. The depletion effect precludes the use of conventional LPCVD for the $SiH_4 + O_2$ reaction. The addition of PH_3 to the gas flow forms P_2O_5, which is incorporated into the SiO_2 film to produce a phosphosilicate glass (PSG)[31]. The reactions are given by:

$$SiH_4 + O_2 \text{ ----------> } SiO_2 + 2H_2 \qquad (5)$$

$$4PH_3 + 5O_2 \text{ ----------> } 2P_2O_5 + 6H_2 \qquad (6)$$

polyhedra have *nonbridging oxygen ions*, which are not shared. The greater the ratio of bridging to non-bridging oxygens, the better the cohesiveness of the glass.

The atomic movement in the glass is more likely to occur by the movement of oxygen atoms rather than silicon atoms, since the rupturing of four Si-O bonds is required to free a silicon atom, while the rupture of only two Si-O bonds are required to free a bridging oxygen atom. If this scission occurs, an oxygen ion vacancy is formed. This vacancy has a net positive charge in the network. Both bridging and nonbridging oxygen vacancies may be formed, but the nonbridging is more likely to occur based on binding energy considerations.

SiO_2 films grown by the oxidation of silicon, have an amorphous structure with a random network of polyhedra. The density of thermally grown fused silica (2.15-2.25 g /cm^3) is less than that of crystalline quartz (2.65 g /cm^3). The lower density implies a more open structure. This open structure is conducive to the interstitial diffusion of impurities through the network.

Impurities introduced into fused silica radically change its properties. As is the case in silicon, both *substitutional* and *interstitial* impurities exist. The substitutional impurities replace silicon in the structure. The most important impurities of this type are boron (B^{3+}) and phosphorus (P^{5+}) ions. Another term for these impurities is *network formers*, since they themselves can be the basis of a glassy structure (B_2O_3 or P_2O_5). The missing or extra electrons in the tetrahedra, when these materials are added, are accommodated by the elimination or formation of bridging oxygen ions, respectively. The elimination of bridging oxygens tend to weaken the network (e.g. boron in SiO_2).

The oxides of Na, K, Pb, and Ba enter the structure as interstitial impurities. When this occurs the metal ion gives up its oxygen to the network, thereby producing two nonbridging oxygen ions,which replaces the original bridging oxygen. The additional nonbridging oxygen also tends to weaken the structure, allowing the glass to be more porous, and thereby increasing the diffusion rate of other species within the glass. Impurity oxides of this type are termed *network modifiers* since they do not form glasses themselves.

Water vapor is a prevalent impurity in fused silica, and can enter from the atmosphere or be grown-in during wet oxidations (or even in so-called dry oxidations, as described in the section entitled: *Oxidation Growth Rates: Water Dependence*). The water vapor combines with a bridging oxygen to form a pair of stable nonbridging hydroxyl groups (OH^-). This reaction can be represented by:

$$H_2O + Si\text{--}O\text{--}Si = Si\text{--}OH + OH\text{--}Si \quad (1)$$

The increase in nonbridging oxygens again tends to weaken the silicon network, thereby increasing the diffusivities of many materials in the network. The presence of OH can be detected by IR spectroscopy, since the Si-OH stretching frequency is different than that of Si-O (resulting in absorption peaks at different wavelengths).

Revesz[2] developed a schematic model (Fig. 1) which shows the fused silica structure, including the presence of the *network formers* (P^{5+}, B^{3+}), the *bridging* and *nonbridging* oxygens, and *network modifiers* (Na^+, K^+, Pb^{2+}, and Ba^{2+}).

OXIDATION KINETICS

Silicon exhibits a propensity to form a stable oxide (SiO_2). Freshly cleaved Si when exposed to an oxidizing ambient (e.g. O_2, H_2O) will form a very thin (<20Å) oxide layer, even at room temperature. When Si is exposed to an oxidizing ambient at elevated temperatures, more rapid growth and thicker oxides are produced.